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2003

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S					FOR APPLICANT	ATTY. DOCKET NO.: YOR920030403USI SERIAL NO.: CONFIRMATION NO. 10/666,353								
INFORMATION DISCLOSURE STATEMENT					· ·	APPLICANT: Chandramouli Visweswariah								
(Use several sheets if necessary)						FILING DATE: HEALWING 9/19/	GROUP: 2825							
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					•	•	OTHER ART (In	cluding Auti	or, Title, Date, Pertinen	t Pages, etc.)				
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/PK/	AK	E	kpli	cit C	omp	utat	ion of Performa	nce as a Fu	nction of Process Va	riation by Lou	Scheffer, TA	U '02, p	p. 1-8 ,	20
/PK/	1 1	Timing Yield Estimation from Static Timing Analysis, by Anne Gattiker, Sani Nassif, Rashmi Dinakar, and Chris Long, pp. 437-442, International Symposium on Quality Electronic Design, 2001.												
/PK/		J. A. G. Jess and C. Visweswariah, "System and method for statistical modeling and statistical analysis of integrated circuits," U.S. Patent Application number 47184,329 filed with the U.S. Patent Office on June 27, 2002.												
XAMINER	/Phallaka Kik/ DATE CONSIDERED 12/01/2007													
						_	whether or not cita		formance with MPEP 609	Draw line thro	igh citation if no	t in confo	rmance and	not

Date Filed: 9/11/2007

PTO/SB/08A (07-05)

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		Application Number	10/666,353			
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	TATEMENT BY APPLICANT	First Named Inventor	Chandramouli Visweswariah			
	(Use as many sheets as necessary)	Art Unit	2641 2825			
		Examiner Name	P. Kik			
Sheet	of 1 2	Attorney Docket Number	YOR920030403US1			

Examiner Initials*	Cite No. ¹	Document Number	U. S. PATENT De Publication Date				
	No.¹	Number-Kind Code ^{2 (# known)} US-	MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Translation	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶	Country
/PK/		THEA2002-279012	09/27/2002	Abstract only		-	Japan
/PK/		PUPA04-274507 JP-04-274567	09/30/1992	Abstract only			Japan

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nder the Paperwork Reduction Act of 1995.	no persons are required to respond to a collection of information unless it contains a walld OMB portral number

Substitute for form 1449/PTO	Complete if Known			
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STATEMENT BY APPLICANT	First Named Inventor	Chandramouli Visweswariah		
(Use as many sheets as necessary)	Art Unit	2041 2825		
(OCCUMENT)	Examiner Name	P. Kik		
Sheet 2 of 2	Attorney Docket Number	YOR920030403US1		

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/PK/		Jess, J.A.G. et al. "Statistical Timing for Parametric Yield Prediction of Digital Integrated Circuits", Proc. Design Automation Conference, ACM,P.932-937, 2-6 June 2003.	
/PK/		Nishimoto Shuji et al., "A Statistical Static Timing Analyzer for CMOS Combinatorial Circuits Considering Correlations Between Delays", Vol.100, No.475 (2000/11/28)pp.11-16, 23 November 2000, English translation of abstract only	•

Examiner	/DI==0=1/21-/	Date	
Signature	. /Phallaka Kik/		12/01/2007
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